A Packaged 2.3 GHz SiGe VCO with Parallel-Branch Inductors

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Abstract — **In this paper, a 2.3 GHz VCO with parallel-branch inductors was designed and fabricated using 0.8-μm SiGe HBT process technology. Their Q-factors were higher than those of the conventional inductors. A good phase noise of –122 dBc/Hz was measured at 4 MHz offset frequency, and harmonics were suppressed by –28 dBc. The manufactured VCO core consumed 3.7 mA at 2 V supply voltage, and the VCO occupied 1.8 mm × 1.2 mm chip areas.**

I. INTRODUCTION

In mobile communication terminals, there have been many requirements such as low cost, high performance and mass production in RF components. Therefore, a number of SiGe transceivers, PLLs, VCOs, LNAs, Mixers, LPAs etc. have been researched and developed as components satisfying those demands. The phase noise of VCO has a significant effect on CDMA systems. So, SiGe device is used as a good candidate for manufacturing an oscillator of low phase noise and low power due to its low turn-on voltage and low 1/f noise [1][2].

In order to increase the quality factor of on-chip inductor and reduce the phase noise of VCO in silicon process, high Q inductors with patterned ground shield and stacked structure have been developed in many papers. This technique improved the quality factor of inductor by 30 % in silicon process [3]. In recently, an improvement of phase noise by increasing maximally the signal power in the resonator has been reported [5]. But since the reported papers use more than two metals, the cost is higher than that of two-metal process. So, in this paper, several parallel-branch inductors with different inner diameters were developed in order to increase the quality factor of inductor with only two-metal layer process and used in this VCO. The proposed parallel-branch inductor showed 12 % improvement in quality factor with the same area as the conventional inductor [6], and the maximum quality factor frequency of the parallel-branch inductor can be tuned by changing the length of the parallel-branch part between first metal and second metal.

In this VCO, a pair of 2.3 nH inductors with inner diameter of 150μm were used, and their maximum quality factors were 9.6 at 4.5 GHz. The packaged VCO had external bonding wires to transfer more output power to the 50 Ω loads, and the measured output powers are –5.4 dBm. The phase noise of the VCO was measured by –122 dBc/Hz at 4 MHz offset carrier, and a current of 3.7 mA at 2 V supply voltage was drawn into the VCO core.

II. SIGE HBT DC AND AC CHARACTERISTICS

Performance parameters of SiGe HBT such as cuff-off frequency (f_T), maximum oscillation frequency (f_{max}), minimum noise figure (NF_{min}) are critically dependent on not only the base thickness, but also the fabrication process. We used RPCVD epitaxial technology to grow base layer, and utilized LOCOS isolation to separate device and device terminals. In this VCO design, their f_T / f_{max} are 41 GHz/42 GHz at V_{CE} = 2V, I_C = 2 mA. In Table 1, the DC and AC parameters of 0.5 × 6.0 μm^2 HBT are summarized.

Table 1. SiGe HBT DC & AC Characteristics

Emitter Area	0.5 × 6.0 μm^2
Beta	296
BV_{EBO} [V]	0.95
BV_{CBO} [V]	10.7
BV_{CEO} [V]	3.5
R_C [Ω]	61
R_E [Ω]	30
f_T [GHz]	41
f_{max} [GHz]	42

III. PARALLEL-BRANCH INDUCTOR

By several reported papers about spiral inductor, series resistance of inductor and substrate resistance are main factors in degrading the Q-factor of silicon inductor [3][4]. In fabricating inductor, 1 μm SiO2 was used between lower and upper metal as a dielectric. The dimensions and specifications of the metal strip and substrate used in

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manufacturing the parallel-branch inductor, are presented in Table 2. Fig. 1 shows the structure of the proposed inductor. The inductor strip starts at the upper metal, branches off in the upper and lower metal strips with the same direction, and terminates at the opposite upper metal. By branching the inductor in parallel with the same direction, the series resistance is reduced, and inductances and parasitic capacitances are added by lower metal. So, the frequency of peak quality factor f_{Qmax} is possible to be tuned, and the higher quality factor can be obtained. Fig. 2 shows the f_{Qmax} of the parallel-branch inductor is lower than the conventional because of additional inductances and capacitances. In Fig. 3, the quality factor is higher because the self and mutual inductances of the lower metal are added and metal resistance R_S is decreased by the parallel branch of the two metal strips. The extracted model parameters and Q-factors of the conventional and parallel-branch inductors versus turn numbers are summarized in Table 3. The values of R_S were reduced.

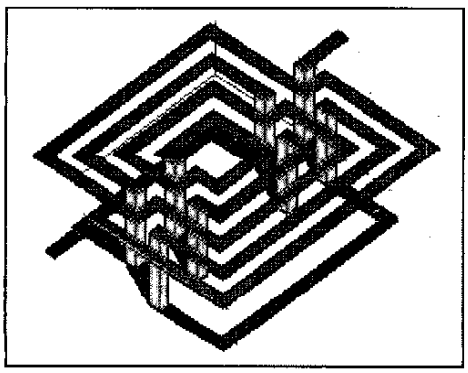

Fig. 1. Parallel-branch inductor structure

Table 2. Dimensions & Spec of the metal and substrate

Sub.Resis [Ω-cm]	Metal	Width (μm)	Space (μm)	Thick. (μm)	Diameter (μm)
5 ~ 15	Al	10	2	1	100

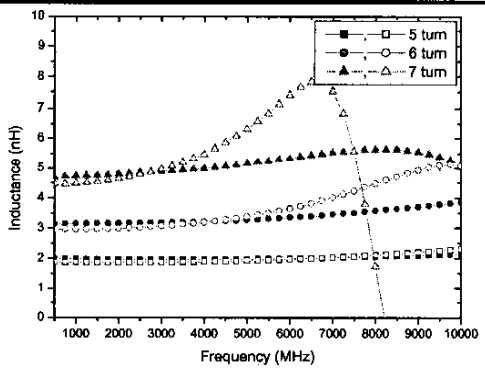

Fig. 2. Inductance of the parallel-branch (vacancy) and the conventional inductor (solid)

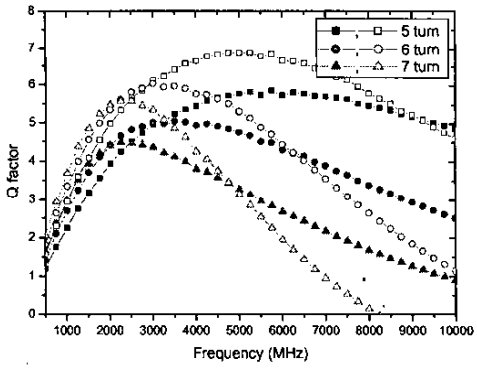

Fig. 3. Q-factor of the parallel-branch (vacancy) and the conventional inductor (solid)

Table 3. Extracted model parameters of two inductors

Param. \ Type	Parallel-branch			Conventional		
Turn num.	5	6	7	5	6	7
Ls (nH)	1.9	2.9	4.4	1.9	3.0	4.7
Rs (Ω)	4.8	5.8	6.7	6.2	8.1	9.0
Cp (fF)	15	30	51	14	19	18
Cox1 (fF)	69	106	210	41	59	200
Cox2 (fF)	257	339	236	284	321	213
Rsub1 (fF)	845	590	581	966	726	727
Rsub2 (fF)	808	602	452	969	844	475
Csub1	12	20	32	3	11	116
Csub2	11	20	16	17	27	30
Q-factor	7.0	6.0	5.6	5.8	5.0	4.5
f_{Qmax} (GHz)	5.0	3.0	2.4	5.8	3.5	2.4

IV. DIFFERENTIAL VCO DESIGN

The full schematic of this VCO is shown in Fig. 4 without varactor diode. The VCO core is composed of the LC tanks and crossed-coupled differential pair negative resistance cell. The parallel-branch inductors in the LC tanks have a diameter of 150 μm with 3 turns, a Q-factor of 8 and an inductance of 2.3 nH at 2.5 GHz.

The variable capacitance for tuning the resonance frequency of the LC tank circuit was implemented by the base-collector and base-emitter junction capacitance of SiGe HBT. In Fig. 5, the measured B-C junction capacitance is shown. The variable capacitance is more increased as the HBTs are more connected in parallel. In this VCO, a pairs of variable capacitors with 12 HBTs connected in parallel were used in symmetry in order to obtain the desired tuning range.

In order to increase the output power of the VCO and isolate the VCO core from the out world, the VCO buffer

of common-emitter type was employed. For the purpose of transferring output power maximally to the load, two capacitors and external bonding wires in packaging the VCO were included in the VCO circuit. The inductance of the external bonding wire is about 1.4 nH. In symmetry, three-transistor current mirrors were used as current sources in order to compensate variations in fabrication process and supply an exact current to the VCO core circuit.

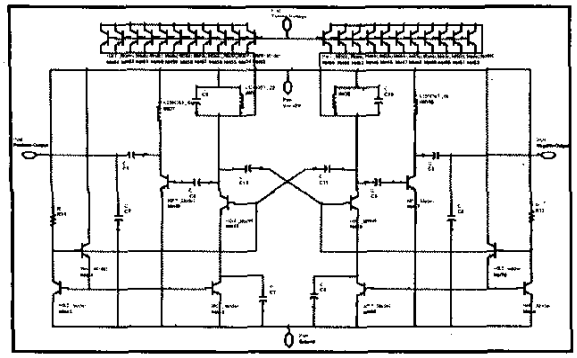

Fig. 4. Full schematic of VCO

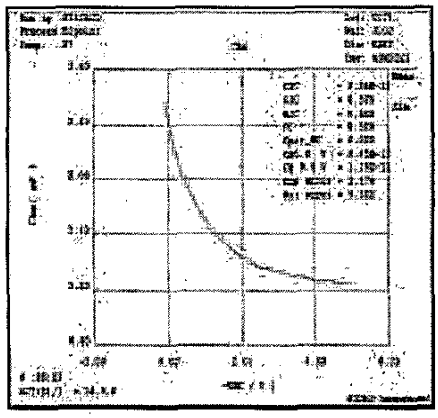

Fig. 5. Base-collector junction capacitance VS voltage

V. MODELING AND SIMULATION RESULTS

The spice Gummel-Poon model was employed in modeling SiGe HBT. Fig. 6 shows the modeled s-parameters fitted to the measured. The s-parameters were measured at V_{CE} of 2 V with a current of 2 mA. From the transient response of Fig. 7, the VCO takes about 15 nsec to reach 90 % steady state. The VCO core consumes 3.7 mA currents at 2 V supply voltage, and a total current of 16 mA are drawn in the whole VCO circuit. The simulated tuning range of the VCO is 2214 MHz ~ 2446 MHz, and the output power is -4.5 dBm, and the phase noise at 4 MHz offset frequency is - 136 dBc/Hz.

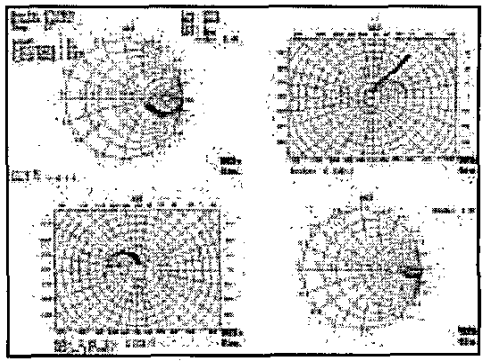

Fig. 6. Comparison between modeled and measured s-parameters

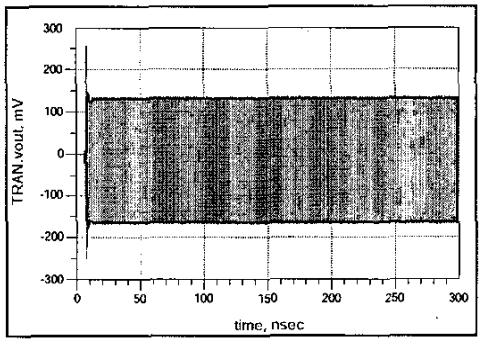

Fig. 7. Transient response of the VCO

VI. FABRICATION AND MEASUREMENTS

We designed and fabricated the VCO circuit using 0.8 μm SiGe HBT process technology. The manufactured VCO photograph is shown in Fig. 8. The chip size is 1.8 mm × 1.2 mm. The inductance of the bonding wire is 1 nH per millimeter. In Fig. 8, the upper center pad is for supply voltage, and the lower center pad is for tuning voltage. The right and left center pads are differential output pads. In Fig. 9, the test jig of the packaged VCO is displayed. The VCO was packaged in commercial Tssop type with 16 pins.

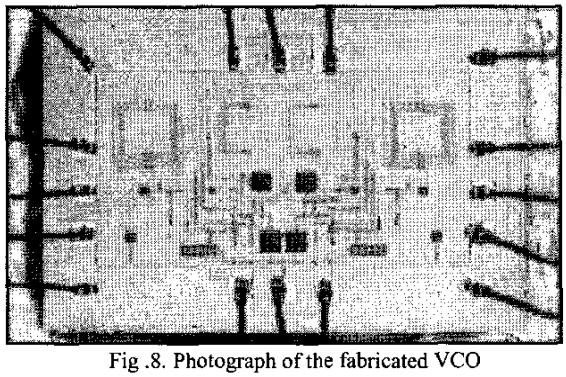

Fig .8. Photograph of the fabricated VCO

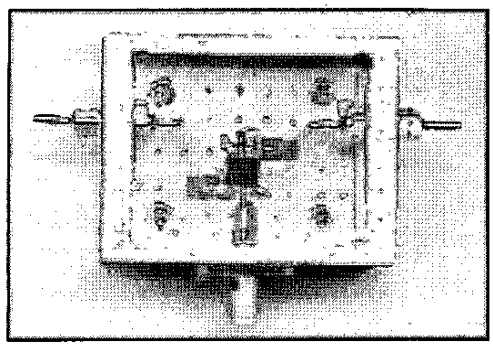

Fig. 9. Test jig with a packaged VCO

The oscillation frequency spectrum is shown in Fig. 10. The output power is -6.4 dBm subtracting the connector and coaxial cable losses of -1.2 dB from the measured output power. A phase noise of -122 dBc/Hz at 4 MHz offset carrier was achieved as shown in Fig. 11. The graph of Fig. 12 represents the measured data comparison between on-wafer and after package. The output power of the packaged VCO was increased by 1 dBm. In Fig. 12, the tuning range after package is from 2165 MHz to 2308 MHz, and the output power is varied from -8.6 dBm to -5.4 dBm. The tuning range shifted down by 50 MHz after packaging. The gain of the VCO is 21 MHz/V.

VII. CONCLUSION

A differential 2.3 GHz VCO with parallel-branch inductor was designed and fabricated using 0.8 μm SiGe HBT process technology. The Q-factor of the parallel-branch inductor was enhanced by 12 %, compared to that of the conventional. A low phase noise at each offset frequency was achieved as shown in Table 4. An external bonding wires in packaging the VCO were used for output matching. A tuning bandwidth of 6.4 % was obtained.

Table 4. Measured Phase Noise

f_{offset}	10 kHz	100 kHz	1 MHz	4 MHz
Pha.N(dBc/Hz)	-100	-108	-115	-122

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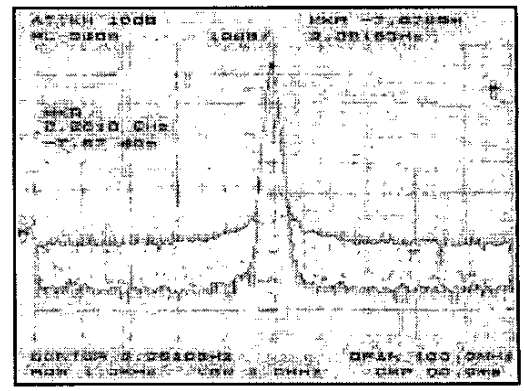

Fig. 10. Oscillation frequency spectrum of the VCO

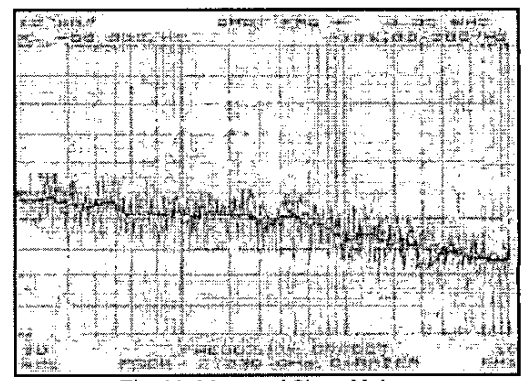

Fig. 11. Measured Phase Noise

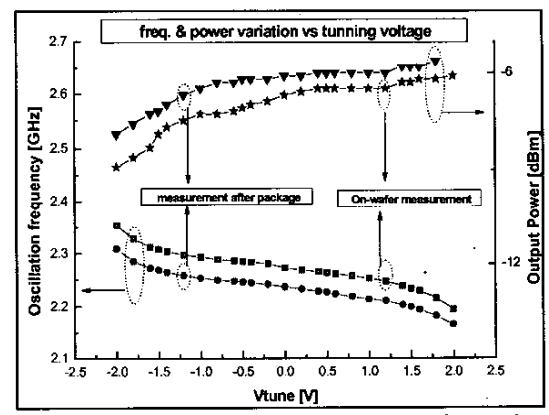

Fig. 12. Measured tuning range after and before package